

Serial No. 10/797081

Attorney Docket No. 01-592

# REMARKS

The applicants note with appreciation the acknowledgement of the claim for priority under section 119 and the notice that all of the certified copies of the priority documents have been received.

The applicants acknowledge and appreciate receiving a copy of the form PTO-1449 that was filed on 11 March 2004, on which the examiner's initials appear next to each cited reference.

Claims 1-12 are pending. Claims 7 and 8 have been withdrawn. Claims 9-12 are new. The applicants respectfully request reconsideration and allowance of this application in view of the above amendments and the following remarks.

The drawings were objected to for failing to show the thin film resistance element through an interlayer insulating film of claim 1. Claim 1 has been amended and now recites a thin film resistance element located above an interlayer insulating film. This is shown in Figs. 1 and 6. Therefore, all features recited in the claims appear in the drawings, and the objection to the drawings should be withdrawn.

Claims 1 and 6 were objected to for the recitation of a thin film resistance element through an interlayer insulating film. As mentioned above, this phrase has been amended, and the objections to claims 1 and 6 should be withdrawn.

Claims 1-5 were rejected under 35 USC 112, first paragraph, as being non-enabling for a taper of zero degrees. Claim 1 has been amended to recite a taper angle that is within a range that is greater than 0° and less than or equal to 10°. This change is considered to overcome the rejection based on the first paragraph of section 112.

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Claims 1, 2 and 4-6 were rejected under 35 USC 103(a) as being unpatentable over Nagao *et al.* (US Pub. 2001/0053559). The applicants respectfully request that this rejection be withdrawn for the following reasons.

Claims 1, 3, and 6 were rejected under 35 USC 103(a) as being unpatentable over Shiiki *et al.* (US Pub. No. 2002/0020879) in view of Nagao *et al.* The applicants respectfully request that this rejection be withdrawn for the following reasons.

Claims 1 and 6 recite the novel embodiment disclosed, for example, on pg. 11, lines 7-12 in which a semiconductor device having a thin film resistance element (30, 200) located above an interlayer insulating film (20, 51) above an area where at least one of an element and a wire (12) is formed on a semiconductor substrate (1) is characterized by a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the thin film resistance element is formed intersects the surface of the semiconductor substrate. The taper angle is set to be greater than zero degrees and less than or equal to 10 degrees.

Nagao *et al.* discloses a process for achieving a high level of flatness for a display device. However, as recited in amended claim 1 and claim 6, in the present invention no flattening process is needed because a step under the resistor is set to be greater than zero degrees and less than or equal to 10 degrees.

The office action states that the film 111 of Nagao *et al.* constitutes a resistor. However, according to Nagao *et al.*, element 111 is a pixel electrode (See paragraph 13). Accordingly, the structure disclosed does not improve deviation of the resistors (referred to as dispersion of pair performance in the specification), unlike the present invention. For this reason, the rejection of

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New claims 10-12 are presented for examination. New claims 10-12 are readable on the elected device of invention I. These claims recite features that further distinguish the present invention from the cited art. Support for new claims 10-12 may be found on, for example, pg. 12.

In view of the foregoing, the applicants respectfully submit that this application is in

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claims 1 and 6 should be withdrawn. Likewise, the rejection of dependent claims 2-4 and 5 should be withdrawn.

The publication of Shiki *et al.* discloses a resistor formed on interlayer film for reducing the semiconductor device surface area. In the publication of Shiiki *et al.*, the interlayer film is flattened and located in the active region. However, the present invention provides the unexpected and superior result of permitting formation of the resistor without the flattening process. Such superior results rebut the examiner's conclusion that one skilled in the art would be motivated to modify the apparatus of Shiki *et al.*

Further, the publication of Shiki *et al.* fails to disclose the recited angle of the step. The publication of Nagao *et al.* was cited to cure this deficiency. However, the publication of Nagao *et al.* also fails to teach or suggest the range being greater than zero degrees and less than or equal to 10 degrees. In response to the examiner's assertion that this range is a result-effective variable, the applicants point out the unexpected and superior results achieved by such a range discussed above.

It is asserted in the office action that it would have been obvious to one of ordinary skill in the art to have modified the apparatus of Shiiki *et al.* by using the method of Nagao *et al.* for obtaining a relatively flat surface without requiring any additional planarization steps such as CMP. The applicants respectfully disagree with this assertion because the publications of Nagao *et al.* and Shiiki *et al.* do not teach or suggest the combination of the resistor and the substantially flat under layer as the interlayer film. Therefore, the rejection of claims 1, 3 and 6 should be withdrawn.

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